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Chavez*

PATENT APPLICATION

Docket No.: 2207/12173

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re the Application of: SOLOMON et al

Group Art Unit: Not assigned

Application No.: Not assigned

Examiner: Not assigned

Filed: September 24, 2001

For: FILTERING BASIC INSTRUCTION SEGMENTS IN A PROCESSOR  
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INFORMATION DISCLOSURE STATEMENT

Director of the U.S. Patent and Trademark Office

Washington, D.C. 20231

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Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The paragraphs marked below are applicable.

1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
2. This Information Disclosure Statement is being filed with a Request for Continued Examination (RCE). No certification or fee is required.
3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

- a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).
- b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).
- c. Please debit Deposit Account No. 11-0600 in the amount of \$240.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.
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- b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

OPTIONAL INSERT PARAGRAPHS FOR INFORMATION DISCLOSURE STATEMENT (Please delete non-applicable paragraphs).

5. Relevance of the non-English language reference(s) is discussed in the present specification.
6. The reference(s) was/were cited in a counterpart foreign application. An English language version of the foreign search report is attached for the Examiner's information.
7. A concise explanation of the relevance of the non-English language reference(s) appears in the Appendix attached hereto.

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PTO/SB/08A (08-00)

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

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Complete if Known

Application Number	Not assigned
Filing Date	September 24, 2001
First Named Inventor	SOLOMON et al
Group Art Unit	Not assigned
Examiner Name	Not assigned

Attorney Docket Number

2207/12173



### U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
		Serial No. 09/735,899		Jourdan et al	Filed 12-14-00	
		5,381,533		Peleg et al	Jan. 10, 1995	

### OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Bellas et al, "Architectural and Compiler Techniques for Energy Reduction in High Performance Microprocessors", <i>IEEE Transactions on VLSI Systems</i> , Vol. 8, No. 3, June 2000	
		Black et al, "The Block-Based Trace Cache", Proceedings of the 26th Intl. Symposium on Computer Architecture, IEEE Computer Society TCCA, ACM SIGARCH, Atlanta, Georgia, May 2-4, 1999	
		Friendly et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", 30th Annual IEEE/ACM Intl. Symposium on Microarchitecture, Research Triangle Park, North Carolina, December 1-3, 1997	
		Intrater et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", 19th Annual Intl. Symposium on Computer Architecture, Gold Coast, Australia, May 19-21, 1992	
		Jacobson et al, "Path-Based Next Trace Prediction", 30th Annual IEEE/ACM Intl. Symposium on Microarchitecture, Research Triangle Park, North Carolina, December 1-3, 1997	
		Manne et al, "Pipeline Gating: Speculation Control for Energy Reduction", Proceedings, 25th Annual Intl. Symposium on Computer Architecture, IEEE Computer Society Tech. Comm. on Computer Architecture, ACM SIGARCH, Barcelona, Spain, June 27-July 1, 1998	
		Glaskowsky, Peter N., "Pentium 4 (Partially) Previewed", <i>Microprocessor Report</i> , Vol. 14, Archive 8, pp. 1, 11-13, August 2000	
		Papworth, David B., "Tuning the Pentium Pro Microarchitecture", <i>IEEE Micro</i> , IEEE Computer Society, Vol. 16, No. 2, April 1996	
		Upton, Michael, "The Intel Pentium® 4 Processor", <a href="http://www.intel.com/pentium4">http://www.intel.com/pentium4</a> , October 2000	
		Rotenberg et al, "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings, 29th Annual IEEE/ACM Intl. Symposium on Microarchitecture, MICRO-29, IEEE Computer Society Tech. Comm. on Microprogramming and Microarchitecture, Assn. for Computing Machinery SIGMICRO, Paris, France, December 2-4, 1996	
		Jourdan et al, "eXtended Block Cache, Proceedings 6 <sup>th</sup> Intl. Symposium on High-Performance Computer Architecture HPCA-6, Toulouse, France, Jan. 8-12, 2000	

Examiner Signature

Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Unique citation designation number.